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Published in:
I E T Power Electronics

Link to article, DOI:
[10.1049/iet-pel.2011.0181](https://doi.org/10.1049/iet-pel.2011.0181)

Publication date:
2012

[Link back to DTU Orbit](#)

Citation (APA):
Zhang, Z., Thomsen, O. C., Andersen, M. A. E., & Nielsen, H. R. (2012). Dual-Input Isolated Full-Bridge Boost DC-DC Converter Based on the Distributed Transformers. *I E T Power Electronics*, 5(7), 1074-1083.
<https://doi.org/10.1049/iet-pel.2011.0181>

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Dual-Input Isolated Full-Bridge Boost DC-DC Converter Based on the Distributed Transformers

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ABSTRACT

In this paper, a new two-input isolated boost dc-dc converter based on a distributed multi-transformer structure which is suitable for hybrid renewable energy systems is investigated and designed. With a novel transformer winding-connecting strategy, the two input ports can be decoupled completely, so the proposed converter can draw the power from the two different dc sources, which have low output voltage, and transfer it to the dc bus, which has high voltage, separately or simultaneously. The detailed operation principles of the proposed converter have been analyzed in the dual-input mode and the single-input mode, respectively. The main advantage of the proposed topology is that the four transformers and the secondary rectifiers are fully utilized whether the converter is connected with two input power sources or only one input. Although the four transformers are employed, the nominal powers of each transformer and rectifier are both reduced by four times. Furthermore, some special issues on converter design, such as increasing number of the input ports, the magnetic integration and the ground loop decoupling are discussed. A 2 kW prototype was built and tested. Experiments on the converter's steady-state and transient operations verified the validity of the analysis and design.

Index Terms— Current-fed, DC-DC converter, isolated, multiple inputs, transformer.

1. INTRODUCTION

Nowadays, clean and renewable energies including fuel cell, wind energy, photovoltaic, etc., have been widely applied to achieve environment friendly objectives [1] [2]. Because of the discontinuity of renewable sources, like wind energy and solar energy, generally, an auxiliary power supply is necessary to

smooth output power and keep output voltage stable under various load conditions. Thus, an efficient combination of different energy sources, to be a hybrid renewable power conversion system, has become an interesting topic [3]. Moreover, high power solar cells or fuel cells are often faced with a need of boosting their low output voltage to a high dc-link voltage subjected to the requirements in grid-connecting applications [4].

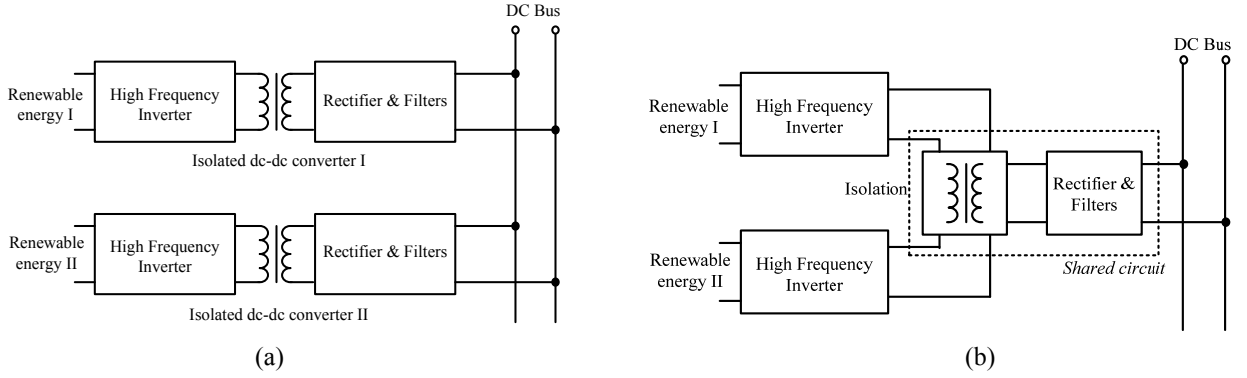


Fig. 1: Block diagram of the systems with two input power sources: (a) Structure based on two isolated individual converters, (b) structure based on the isolated multiple-port structure.

In the last decade, various hybrid system structures have been proposed. For the applications with galvanic isolations, basically, high frequency isolated converters with different input sources can be connected in parallel on a mutual dc bus and thereby each sub-converter can be designed as an individual power module. The block diagram of this system is shown in Fig. 1 (a). The main disadvantage of this system is that if one input source is connected, only one converter will be operated and the other one will be completely under the idle condition that will reduce the power density of the whole system. Due to this reason, multi-port converters have been proposed and received more and more attention in recent years. In these topologies, some parts of the dc-dc converters (such as rectifiers and filters) can be utilised by different input ports mutually, as shown in Fig. 1 (b). Although it will cause complex system control, the power density of the system can be increased in some applications. A three-port series resonant converter operating at constant switching frequency was proposed in [5], which can achieve soft-switching and high frequency operation. After that, a modelling and control method based on this resonant multi-port converter was investigated in [6]. With a systematic approach [7], [8], an isolated single primary winding multiple-

input converter which combined a two-input buck converter and a flyback converter was studied in [9]. By applying a concept of dual active bridge (DAB) converter [10] [11], multiple-port bidirectional converter topologies employing multiple transformer windings were proposed in [12], where the separate windings are used for each port and the bidirectional power flow is easily controlled by a phase-shift angle and/or duty cycle [13]. Based on a current-fed half-bridge structure proposed in [14], the characteristics of triple-port half-bridge were studied in [15] and [16]. As the conclusion given in [17], for the sustainable energy with a low output terminal voltage such as fuel cell, a boost-type converter is favorable for a high efficiency operation. A multi-input isolated boost dc-dc converter with multi-windings based on the flux additivity concept was proposed in [18], but the reverse current block diode is connected in series with the MOSFETs on the primary side, which makes the bidirectional power flow impossible, so the auxiliary circuit for rechargeable elements is needed. In [19], a high step-up isolated converter with two input sources was investigated, and the converter utilizes the current-source type applying to both of the input power sources. To avoid the switch voltage spikes caused by the leakage inductor, an active clamping circuit is added.

The aim of this paper is to investigate an innovative dual-input full-bridge isolated dc-dc converter [20] for a hybrid renewable energy system. With the novel winding connection and the interleaved PWM modulation strategy, two current-fed power sources with low input voltage can deliver the power to the high voltage dc bus or the load, individually or simultaneously. In this paper, firstly, a review on the state of the art of the multiple-input isolated converters is given to express the background and novelty of this research work. Then, based on the proposed topology, a detailed analysis of the steady-state operation principles of the converter is given and hereby the characteristics of the converter are explained in depth. In order to improve the converter performance further, some issues such as the input port extension, the magnetic integration and the common mode current deduction, which affect the hardware design in practice, are discussed, and some possible solutions are presented. The operating performance of the proposed dual-input converter is examined and is validated through some computer simulations. Finally, a laboratory

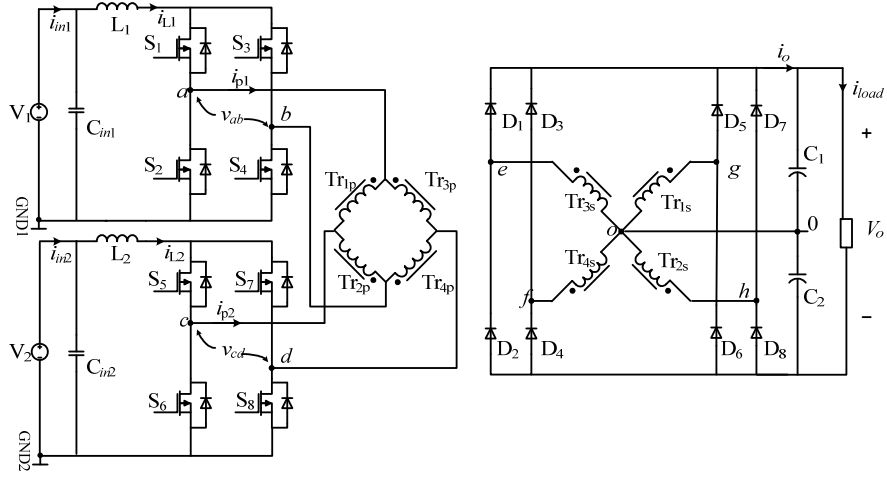
experimental prototype was set up to verify this new dual-input isolated boost converter. Using the above study procedure, the salient features of the proposed converter can be summarized: a high step-up ratio, an electric isolation between the clean energy and output voltage, multiple input power sources, and magnetic integration. The structure of this paper is organized as follows. Following the introduction, the topology and operation principle of the proposed converter are presented in Section 2. In Section 3, the special issues on the converter design are discussed. The hardware design and the experimental results are provided in Section 4. Finally, the conclusion is drawn in Section 5.

2. BASIC PRINCIPLE AND STEADY-STATE OPERATION

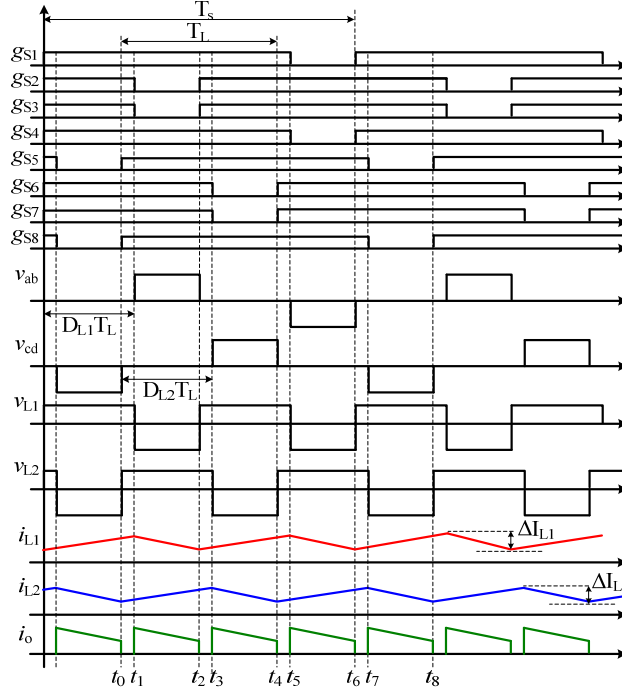
As shown in Fig. 2 (a), the proposed dc-dc converter consists of two boost inductors, two high frequency full-bridge inverters, four transformers and a common output-stage circuit. It is driven by two dc voltage sources, that when associated with large inductors become dc current sources. $Tr_1 \sim Tr_4$ are four identical transformers with same number of turns and turns ratio. According to the converter's operation, its operating principles can be analysed with two different modes: dual-input mode and single input mode.

2.1 Dual-Input Mode

The timing diagrams and the basic operating waveforms in this mode are shown in Fig. 2 (b). There is 180° phase shift between each pair of drive signals, namely S_1, S_4 and S_2, S_3 . The switches S_5 to S_8 have the same operating principle with that of S_1 to S_4 . It is worth noting that when the switches in the diagonal position in one of the H-bridges form a simultaneous conduction switch pair to transfer power to the secondary side, it will cause every transformer winding current on the primary side to be clamped as I_{L1} or I_{L2} . The appearance of the clamped current will disable the normal operation of the other dc input-stage circuit, because the current sources can not be connected in series, which means two input ports can not transfer power at same time. To solve this problem, the phase-shift PWM scheme is utilized, which gives 90° phase shift between S_1 and S_5 . With that, the two input power sources can deliver power to the secondary side simultaneously. Due to the symmetry of the switching mechanism, only the operating principles of the proposed converter in a half switching period are analysed below.



(a) the proposed converter topology



(b) Timing diagrams of the basic operating waveforms in steady state

Fig. 2: Topology and operation of the proposed dual-input isolated boost converter.

In subinterval (t_0-t_1) , all the eight primary side switches operate in their ON states. As shown in Fig. 3 (a), the inductors L_1 and L_2 connect across the dc input sources V_1 and V_2 , respectively. With primary and secondary coils shorted, all the diodes on the secondary side are reverse-biased. Here, two input inductors are charged by the input sources and no power is delivered to the secondary side. Thus, the load current is provided by the output capacitors C_1 and C_2 . The primary inductor currents $i_{L1}(t)$ and $i_{L2}(t)$ can be expressed respectively as

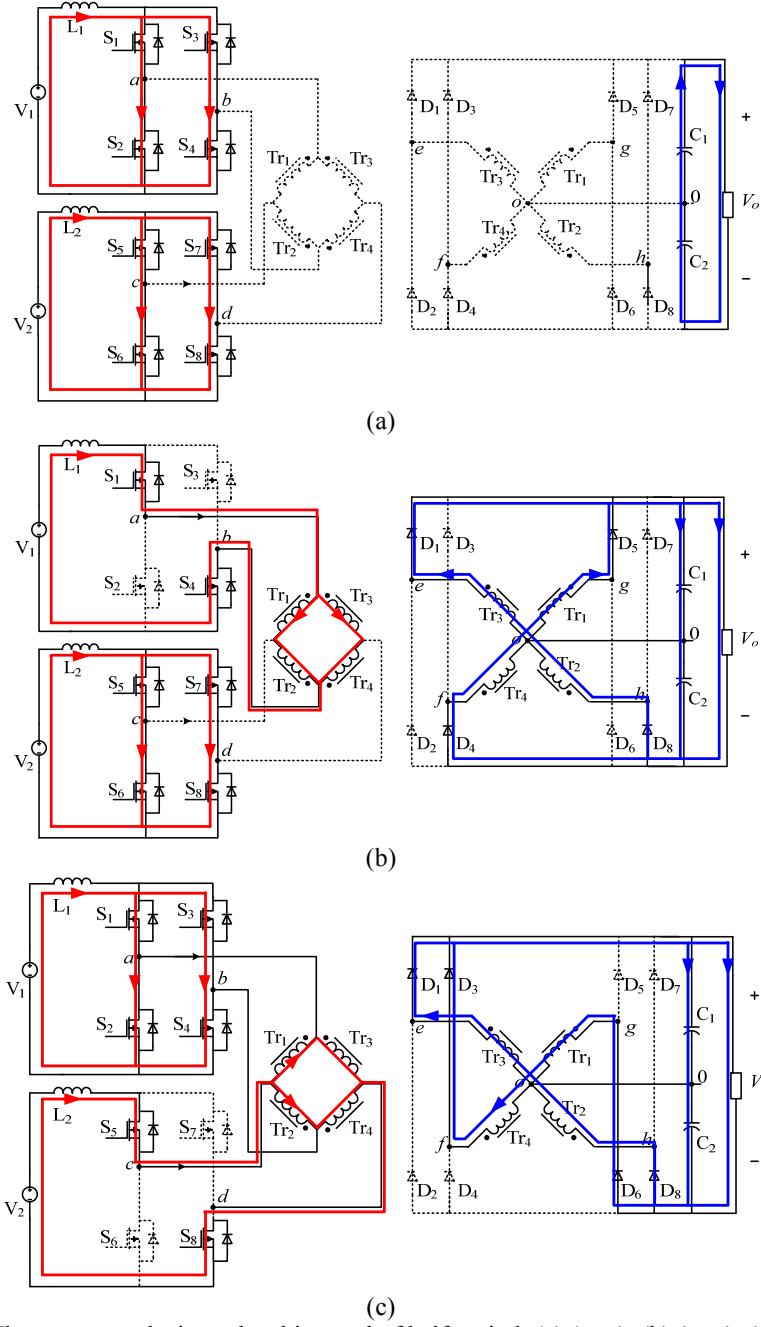


Fig. 3: The current paths in each subinterval of half period: (a) (t_0-t_1) ; (b) (t_1-t_2) ; (c) (t_3-t_4) .

$$i_{L1}(t) = (I_{L1} + 0.5\Delta i_{L1}) + \frac{V_1}{L_1} \cdot (t - t_1) \quad (1)$$

$$i_{L2}(t) = (I_{L2} - 0.5\Delta i_{L2}) + \frac{V_2}{L_2} \cdot (t - t_0) \quad (2)$$

During the second subinterval (t_1-t_2) , S_2 and S_3 operate in their OFF states so that the inductor L_1 is connected via the transistors S_1 and S_4 through the paralleled paths: one is Tr_1 in series with Tr_2 and the

other one is Tr_3 in series with Tr_4 . On the secondary side, the diodes D_1 , D_4 , D_5 , and D_8 are forward-biased to carry the output current. Thus, v_{ab} is clamped to V_o/n , and v_{cd} is clamped to 0, where n is the turn ratio of transformer. The current paths are plotted in Fig. 3 (b). $i_{L2}(t)$ can be expressed as same as that in subinterval (t_0-t_1) , and $i_{L1}(t)$ is calculated by

$$i_{L1}(t) = (I_{L1} + 0.5\Delta i_{L1}) + \frac{\left(V_1 - \frac{V_o}{n}\right)}{L_1} \cdot (t - t_1) \quad (3)$$

In subinterval (t_2-t_3) , all the switches on the primary side are turned on, so the operation principle is same to that in (t_0-t_1) and the equivalent current paths can also be illustrated by Fig. 3(a).

During the subinterval (t_3-t_4) , S_6 and S_7 operate in their OFF states so that the inductor L_2 is connected via the transistors S_5 and S_8 through the paralleled paths: one is Tr_2 in series with Tr_4 and the other one is Tr_1 in series with Tr_3 . On the secondary side, the current flows through the diodes D_1 , D_3 , D_4 and D_8 to the dc output, as shown in Fig. 3 (c). So v_{cd} is clamped to V_o/n and v_{ab} is clamped to 0. $i_{L1}(t)$ and $i_{L2}(t)$ are given,

$$i_{L1}(t) = (I_{L1} - 0.5\Delta i_{L1}) + \frac{V_1}{L_1} \cdot (t - t_2) \quad (4)$$

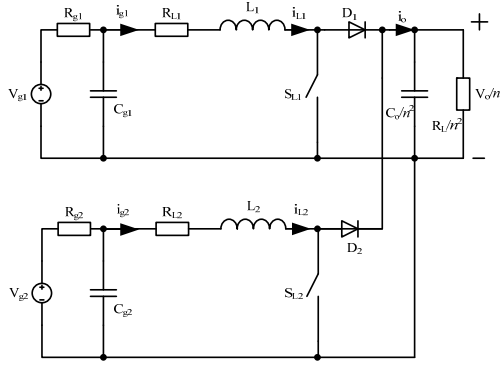
$$i_{L2}(t) = (I_{L2} + 0.5\Delta i_{L2}) + \frac{\left(V_2 - \frac{V_o}{n}\right)}{L_2} \cdot (t - t_3) \quad (5)$$

Having described the subintervals in a half period, the operating principle of each subinterval in the second half period is similar. Furthermore, based on the analysis above, during the positive half switching period, the converter can be simplified and shown in Fig.4 (a), where R_g and R_L are the series resistance of the power source and the boost inductor. According to the plot shown in Fig. 4 (b) and the analysis results in [21], here the corresponding inductor duty cycle, D_{Li} ($i=1, 2$), and inductor period time T_L are defined as

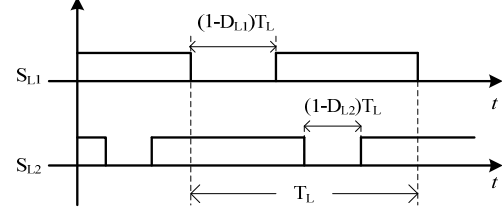
$$D_{Li} = 2D_{si} - 1 \quad (i=1,2) \quad (6)$$

$$T_L = T_s / 2 \quad (7)$$

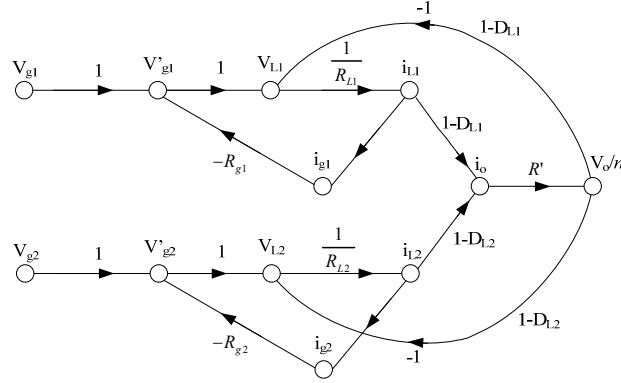
where D_s ($0.5 \leq D_s \leq 1$, theoretically) is the switching duty cycle and T_s is the switching period.



(a) Equivalent circuit of the proposed converter ;



(b) Equivalent driving signals;



(c) The steady-state model of the proposed converter.

Fig. 4: Equivalent circuit and steady-state model of the converter in the positive half switching period.

Hence the steady-state model for the proposed converter is obtained by the flow-graph nonlinear modelling technique [22], which is plotted in Fig.4 (c). Neglecting all the parasitic parameters, the open-loop voltage gain of this converter can be derived as

$$\frac{V_o}{V_1} = \frac{n}{1 - D_{L1}} \quad (8)$$

$$\frac{V_o}{V_2} = \frac{n}{1 - D_{L2}} \quad (9)$$

From (8) and (9), clearly, the proposed converter can be completely decoupled into two independent isolated boost converters based on the utilized winding connection and the interleaved PWM modulation strategy. Neglecting all the losses, the output power P_o is the summation of the input power P_1 and P_2 and can be expressed as

$$\begin{aligned} P_o &= P_1 + P_2 \Leftrightarrow \\ V_o I_o &= V_1 I_1 + V_2 I_2 \end{aligned} \quad (10)$$

As a result, the output current can be determined by

$$I_o = \frac{1-D_{L1}}{n} \cdot I_1 + \frac{1-D_{L2}}{n} \cdot I_2 \quad (11)$$

The derived large-signal, small-signal and steady-state models of the proposed converter as well as the detailed design procedure of the voltage and current closed-loop controllers can be found in [23].

2.2 Single-Input Mode

The single-input mode can be seen as a special condition of the double-input mode and its equivalent circuit is shown in Fig. 5. The operation principle in single-input mode is similar to that of the conventional isolated boost converter with H-bridge input circuit [24]. In order to ensure the ON states of the switches overlap, the switch duty cycle D_s has to be bigger than 0.5. Hence there is a continuous current path for the inductor L_1 . The conversion ratio of the converter in the continuous current mode (CCM) is

$$\frac{V_o}{V_1} = \frac{n}{1-D_L} = \frac{n}{2(1-D_s)} \quad (D_s \geq 0.5) \quad (12)$$

As we can see, all the four transformers can also be utilized completely in the single-input mode. Hereby, the proposed converter has the potential ability to achieve high power density, in comparison to the system consisting of two individual isolated boost converters in parallel. This is true especially for high power applications, where the main power stage is fully used both in dual-input and single-input conditions.

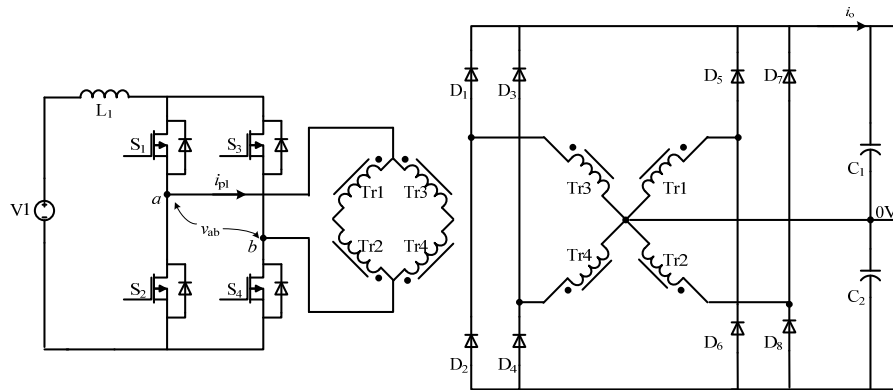


Fig. 5: The equivalent circuit in single-input mode of the converter.

3. SPECIAL ISSUES ON THE CONVERTER DESIGN

To improve the performance of the proposed dc-dc converter, some practical issues such as how to reduce the inductive elements, extending the number of inputs and common mode current deduction are discussed below.

3.1 Magnetic Integration

The complex winding connection makes an optimal layout of the primary side difficult. But by an effective magnetic integration, the number of the inductive elements can be reduced [25]. In the dual-input mode, the voltages across every primary winding are listed in Table 1.

Table 1 Voltages across each primary winding

| Subintervals | v_{Tr1a} | v_{Tr2a} | v_{Tr3a} | v_{Tr4a} |
|--------------|------------|------------|------------|------------|
| (t_1-t_2) | $+V_O/2n$ | $-V_O/2n$ | $+V_O/2n$ | $-V_O/2n$ |
| (t_3-t_4) | $-V_O/2n$ | $-V_O/2n$ | $+V_O/2n$ | $+V_O/2n$ |
| (t_5-t_6) | $-V_O/2n$ | $+V_O/2n$ | $-V_O/2n$ | $+V_O/2n$ |
| (t_7-t_8) | $+V_O/2n$ | $+V_O/2n$ | $-V_O/2n$ | $-V_O/2n$ |

It can be seen that windings Tr_{1a} and Tr_{4a} as well as Tr_{2a} and Tr_{3a} always have opposite voltage. In order to reduce the transformer footprint area and increase the power density, the two input inductors L_1 and L_2 , and the four individual transformers, Tr_1 , Tr_4 , and Tr_2 , Tr_3 , can be wound with two sets of E-I-E cores, shown in Fig. 6 (a). The windings of each transformer are equally divided into the outer legs of E-cores. In transformer Tr_1 , $P_1/2$ and $S_1/2$ represent the half of primary winding and the half of secondary winding respectively. $P_4/2$ and $S_4/2$ are the same properties for the transformer Tr_4 . L_{1-1} in parallel with L_{1-2} wound in the center legs of E-cores to form the boost inductor L_1 . The middle I-core provides a shared flux return path. ϕ_1 and ϕ_4 represent ac flux generated by the transformers Tr_1 and Tr_4 respectively.

By arranging the directions of the windings on the outer legs for each transformer, zero ac flux can be achieved in the centre legs. ϕ_1 and ϕ_4 have their own flux paths due to a low reluctance path provided by shared I-core meaning the two transformers Tr_1 and Tr_4 are uncoupled. Because ϕ_1 is equivalent to ϕ_4 in this work, the ac flux will partially cancel in shared I-core. The dc flux ϕ_{L1} generated by the inductor L_1 goes

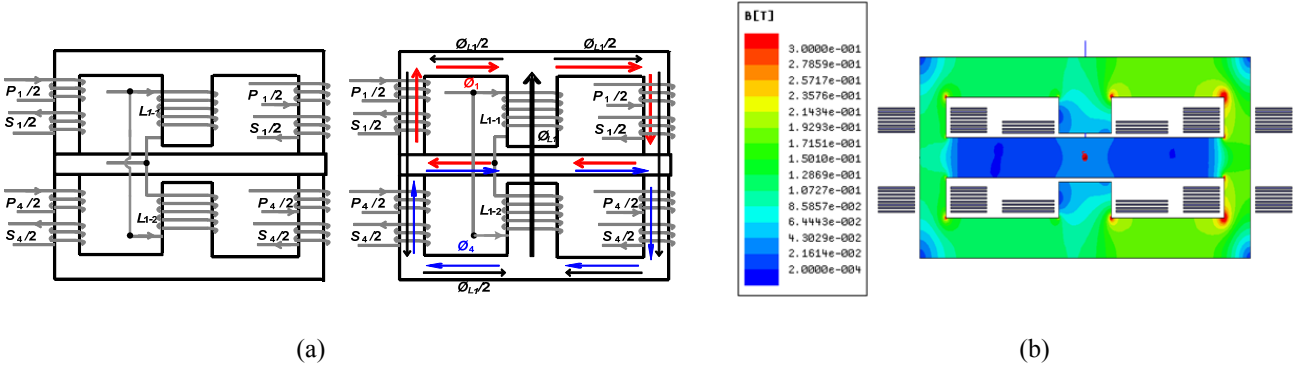


Fig. 6: Two transformers and one input inductor in E-I-E integration, (a) winding arrangement; (b) 2D simulation by FEA analysis.

through the centre legs of E cores. Half of \mathcal{O}_{L1} runs in the outer legs of the E-cores and no dc flux exists in the shared I-core due to complete cancellation effect. To verify the validity of the proposed design approach and theoretical analysis, a 2D simulation model linked with external circuit has been built in a finite element analysis (FEA) tool. As shown in Fig. 6 (b), the right side has higher flux density B because half of \mathcal{O}_{L1} adds to \mathcal{O}_1 and \mathcal{O}_4 but on the left side, these fluxes subtract. In the shared I core, \mathcal{O}_1 and \mathcal{O}_4 cancels out. Hence, based on this magnetic integration idea, the four transformers and two inductors can be integrated into two sets of E-I-E cores. It reduces the number of magnetic elements as well as the core losses. More detailed design procedure can be found in [25].

3.2 Method to Increase the Number of Inputs

The primary and secondary windings of the transformers from the Fig. 2 are re-illustrated in Fig. 7(a). The voltage vector across the different terminals, from a to d on primary side, and the current vectors, from e to h on secondary side can be plotted in Fig. 7 (b), where the employed primary windings are numbered as 1~4. According to the operating sequence, the potential and current vectors will rotate clockwise like a 2-pair-pole dc motor. Based on this simplified model, the other 2-pair poles can be added symmetrically in the system with a phase shift: 45 degree electrical angle, as shown in Fig. 7 (c), and thereby the proposed dual-input converter can be extended to a converter with 4 input ports by the winding connection shown in Fig. 7 (d). Thus, the number of inputs N_{input} and the corresponding number of transformer N_{Tr} can be derived as

$$N_{input} = 2^m \quad (m = 1, 2, \dots)$$

$$N_{Tr} = 2N_{input}$$
(13)

The constraint on inductor duty cycles is expressed as

$$D_{L1} + D_{L2} + \dots + D_{LN} \geq 1$$
(14)

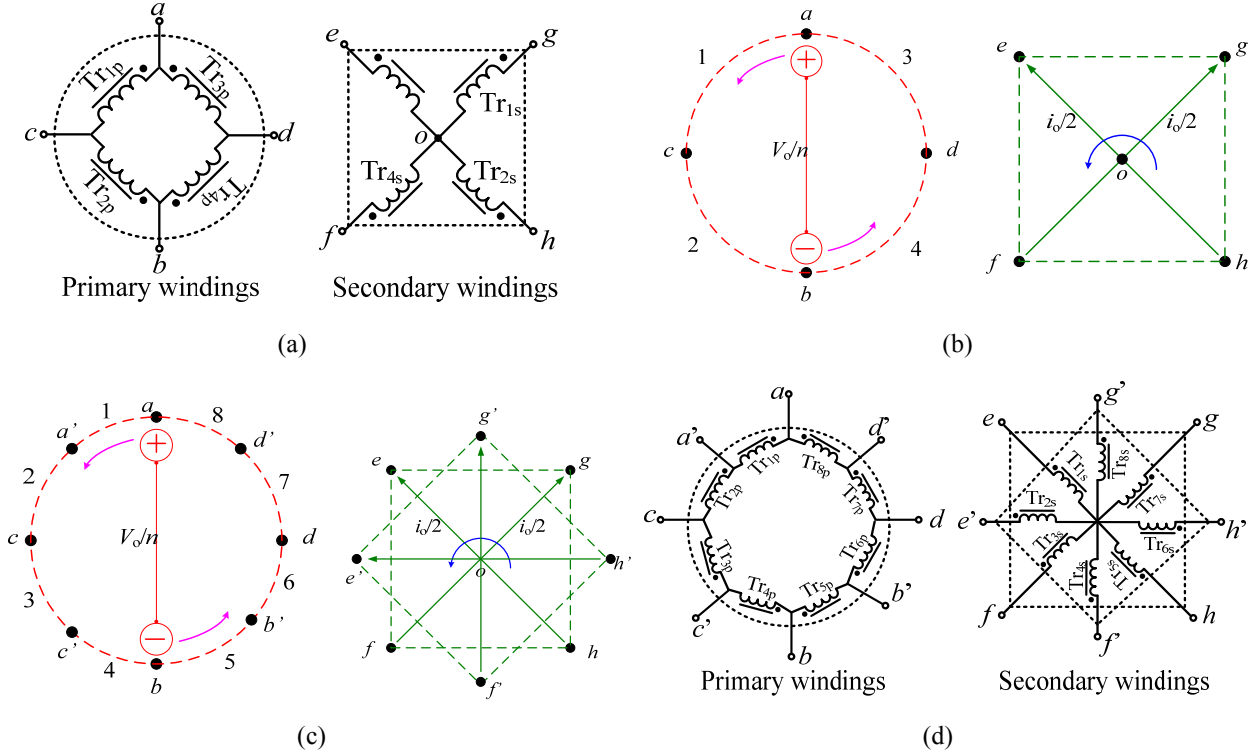


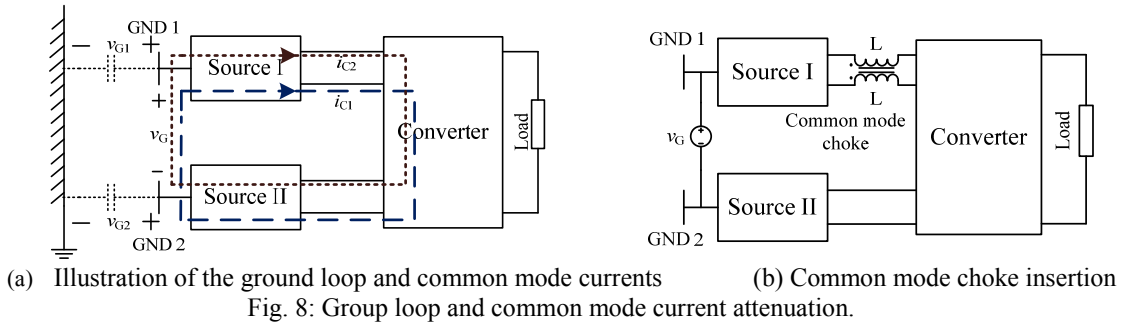
Fig. 7: Method to increase the number of inputs: (a) windings for two inputs, (b) equavilent voltage and current vectors for two inputs, (c) equavilent voltage and current vectors for four inputs, (d) windings for four inputs.

It is worth noting that: 1) the number of inputs must be exponent of 2; 2) with increasing number of input ports, the number of the transformers is increased by twice that of input ports. If the converter has multiple inputs, utilizing the high order magnetic integration method can simplify the converter circuit further, but it is out of scope of this paper and will not be discussed here.

3.3 Ground Loop and Common Mode Current Attenuation

According to the operation principles described in Section 2, the two input ports cannot be connected at one common ground point; otherwise two primary windings will be shorted by the ground that will reduce the power delivery capability. The different potentials between two ground systems can result in a serious

interference problem in high frequencies, where ground loops are induced if the coupling capacitors exist between two different power returns as shown in Fig. 8 (a). Furthermore, the common mode currents (i_{C1} and i_{C2}) caused by the ground loops are quite large because the output capacitors C_1 and C_2 have very low impedance as seen from the primary side. There are several methods for blocking this path. In this paper, the more common and easily implemented method is used: a common mode choke is inserted at the input return wires to attenuate the common mode current flowing through the two input ports as shown in Fig.8 (b).



4. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a laboratory prototype of the proposed converter with 4 individual transformers is implemented and tested, which is shown in Fig. 9. The specifications and component details of the tested prototype are given in Table 2.

Table 2 Specifications and component details of the tested prototype

| | |
|---------------------------------------|---|
| Rated input voltage, V_1 and V_2 | 30 – 60 VDC |
| Rated output voltage, V_o | 400 VDC |
| Rated output power, P_o | 2 kW |
| Switching frequency, f_s | 50 kHz |
| Boost inductors, L_1 and L_2 | 22 μ H, N87 ferrite core, copper foil winding |
| Input filter, C_{in1} and C_{in2} | 10 μ F/250V Film Cap: 2 in parallel |
| Output filter, C_1 and C_2 | 6.8 μ F/250V Film Cap: 4 in parallel |
| MOSFETs S_1 - S_8 | IRFP4568, 150V/171A |
| Diodes D_1 - D_8 | HFA15TB60, 600V/15A |

To achieve low profile and high power density, planar transformers utilizing planar windings instead of the traditional windings made of Cu -wires are designed for this work. The transformer turns ratio is:

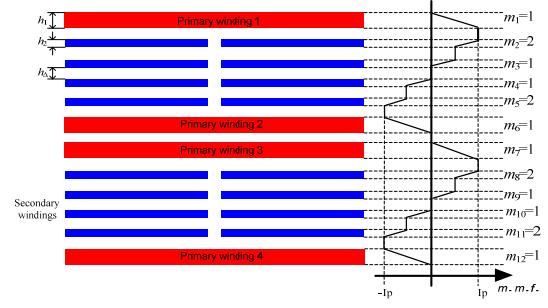
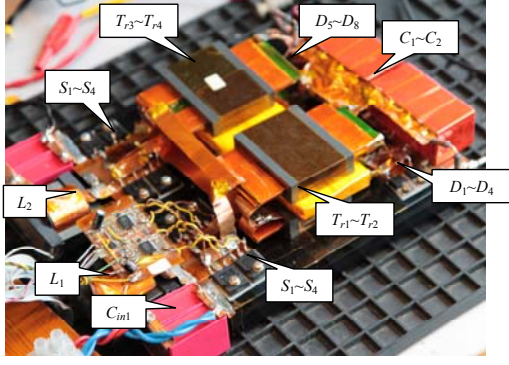


Fig. 9: Experimental prototype of the proposed two-input converter. Fig. 10: Interleaving transformer-winding configuration.

$N_p/N_s=1:4$. In order to reduce the ac resistance and leakage inductance of transformer, the interleaving structure is utilized as winding arrangement. Considering the electromagnetic interference problem, the size of the core and the PCB winding thickness, in this design, the primary windings (P) and the secondary windings (S) are arranged as $P-8S-2P-8S-P$ as shown in Fig. 10. Each primary winding is wound with 0.2 mm copper foil and double-layer 50 μm Kapton tape as an isolator between the windings. The 16-turn secondary winding is realized by two 4-layer PCB boards, and each board contains 8-turn with 1 oz copper thickness. The ac resistance and leakage inductance can be calculated by (15)-(17), where ξ is conductor height in penetration depth at fundamental frequency, m is number of layers in winding portion, F is magneto motive forces, l_w is mean turn length and b_w is width of winding.

$$R_{ac} = \frac{\xi}{2} \left[\frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m-1)^2 \cdot \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right] \cdot R_{dc} \quad (15)$$

$$m = \frac{F(h)}{F(h) - F(0)} \quad (16)$$

$$\begin{aligned} L_{lk} &= \frac{\mu_0 \sum \int_0^h (H^2 \cdot l_w \cdot b_w) \cdot dx}{I_p^2} \\ &= \mu_0 l_w b_w \left[4 \int_0^{h_1} \left(\frac{x}{h_1 b_w} \right)^2 dx + 8 \int_0^{h_2} \left(\frac{x}{2h_2 b_w} \right)^2 dx + 4 \left(\frac{1}{b_w} \right)^2 h_{\Delta} + 4 \left(\frac{1}{2b_w} \right)^2 (h_2 + h_{\Delta}) \right] \\ &= \frac{l_w}{3b_w} \cdot (4h_1 + 5h_2 + 15h_{\Delta}) \end{aligned} \quad (17)$$

The magnetizing inductance, ac resistance and leakage of each transformer are also measured by PSM1735 impedance analyser. The measurement results and calculated results (T_{cal}) are listed in Table 3.

Table 3 Measurement results of the transformers

| (@ 50 kHz) | Magnetizing inductance (μH) | Leakage inductance ($n\text{H}$) | ac /dc resistance ($m\Omega$) |
|-------------|--|------------------------------------|---------------------------------|
| Tr_1 | 242.1 | 52.0 | 22.6/20.5 |
| Tr_2 | 245.0 | 53.1 | 23.4/21.1 |
| Tr_3 | 241.5 | 53.5 | 23.0/21.0 |
| Tr_4 | 240.4 | 52.2 | 22.9/20.9 |
| T_{cal} | 260.0 | 47.5 | 20.3/20.1 |

The MOSFETs on primary side must block the reflected load voltage $V_o/n=V_1/(1-D_{L1})=V_2/(1-D_{L2})$. As to the influence of the leakage inductance on the switching devices, that is an issue limiting the application of an isolated full-bridge boost converter, the analysis of transformer leakage inductance in [21] reveals that a low leakage inductance can be achieved by interleaving arrangement of transformer windings, allowing stored energy to be dissipated. Power MOSFETs fully rated for repetitive avalanches allow primary-side voltage clamp circuits to be eliminated. Here the transformers with low leakage inductance are utilised, so over sizing of the primary-switch voltage rating and any clamp circuits can thus be avoided. On the secondary side, the block voltage of $D_1\sim D_8$ is V_o , which is clamped by the output voltage naturally. IRS2110 is used as the gate driver together with ISO722C capacitive digital isolators for control signal protection. The control signals are generated by a TMS320F2808 digital signal processor. To minimize the ac loop, C_1 and C_2 are placed close to the diode rectifiers.

Fig. 11 shows Simulink/PLECS simulation results. Simulation parameters are based on the above design parameters ($V_1=V_2=30\text{V}$ and $V_o=400\text{V}$). The simulation results in Fig. 11 agree with the theoretical analysis described in section 2.

The experimental waveforms are shown in Fig. 12. In the single input mode with 50 V input voltage, Fig. 12(a) shows the primary side voltage and current, i.e. v_{ab} and i_{p1} , which have been annotated in Fig. 2. While Fig. 12(b) shows the plots of the primary voltages v_{ab} and v_{cd} , and primary current i_{p1} and i_{p2} in the dual-input mode with the conditions: $V_1=50\text{ V}$ and $V_2=30\text{ V}$, which verifies the theoretical analysis results

that two input voltage sources can deliver the power together. It is clear that a phase-shift angle exists between the two high frequency ac voltage waveforms.

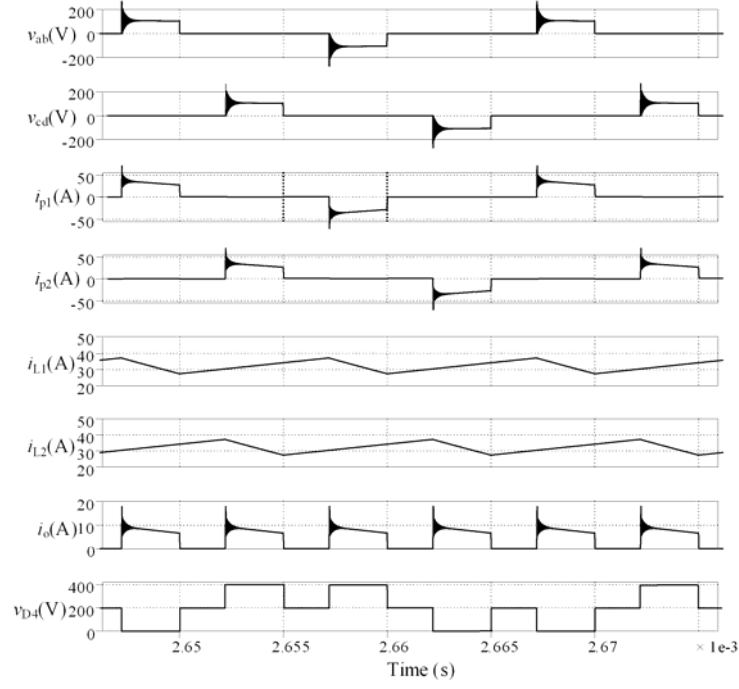
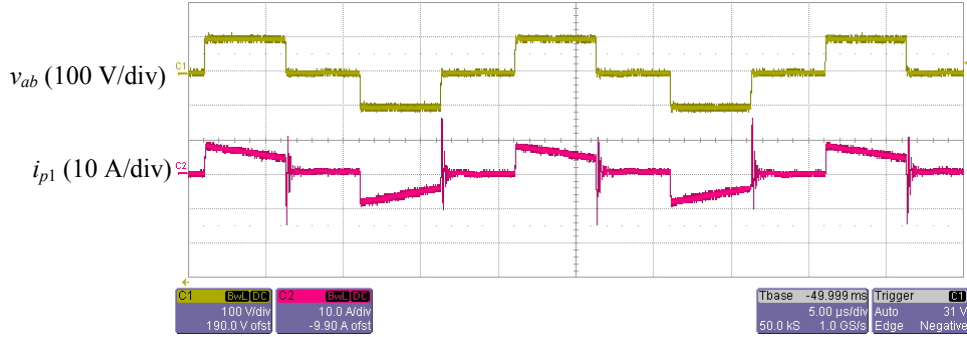
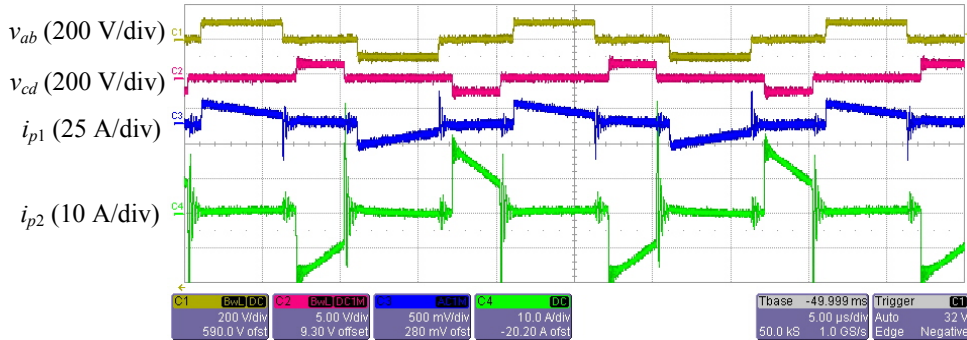


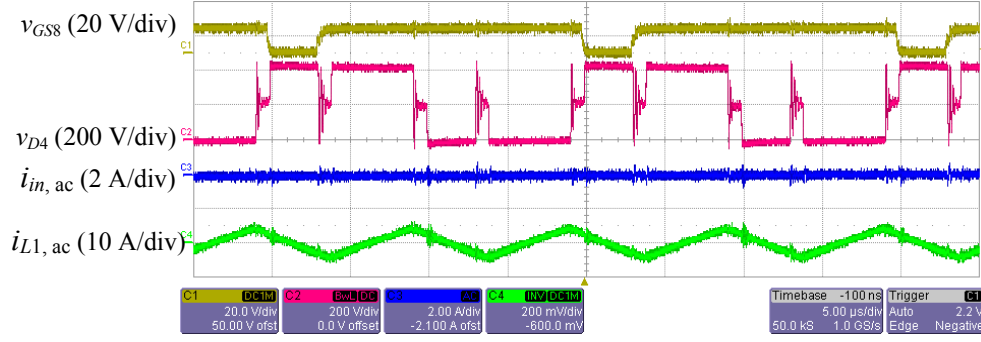
Fig. 11: Simulation results: v_{ab} , v_{cd} , i_{p1} , i_{p2} , i_{L1} , i_{L2} , i_o and v_{D4} .



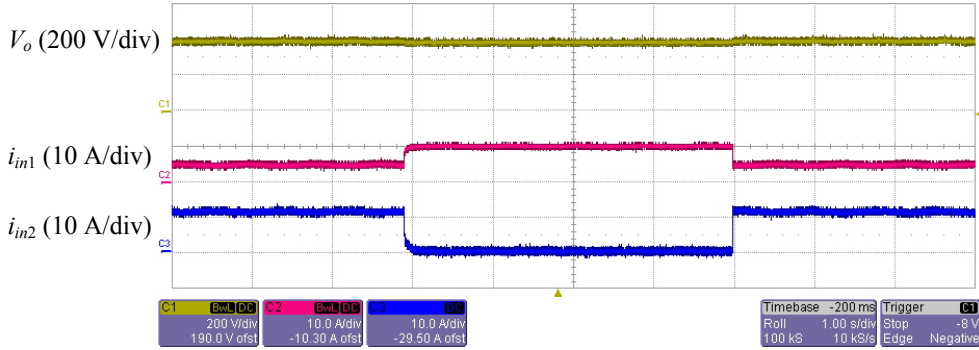
(a) Primary side voltage and current under single-input mode (time base: 5 us/div)



(b) Primary side voltages and currents under dual-input mode (Time base: 5 us/div)



(c) Drive signal of S_8 (v_{GS8}), voltage across the diode D_4 (v_{D4}), ac input current ($i_{in, ac}$), and ac current flowing through input inductor (i_{L1ac}) under dual-input mode (Time base: 5 μ s/div)



(d) Transient response when $V_1=50$ V and $V_2=30$ V. (Time base: 1s/div)

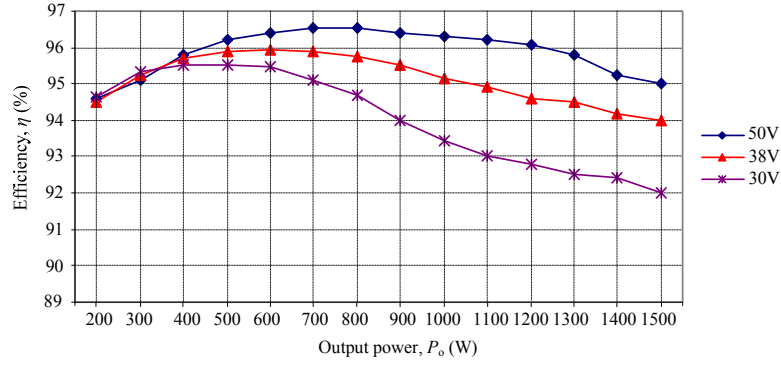
Fig. 12: Experimental waveforms of the proposed converter.

In Fig. 12(c), the experimental waveforms of drive signal of S_8 (v_{GS8}), voltage across the diode D_4 (v_{D4}), ac input current ($i_{in, ac}$), and ac current flowing through input inductor (i_{L1ac}), are presented. Because of boost-type converter, the diode voltage is clamped by the output voltage without any voltage spike and although only the film capacitors are used as the input filter, the input current ripple $i_{in,ac}$ is still very small. It can be seen that with the inserted common mode chock there is no resonance voltage, so the ground loop is decoupled. Fig. 12(d) shows the output voltage V_o and two input currents i_{in1} and i_{in2} , when the operating mode is switched from single input to dual input and then back again under the constant output power condition. So it is clear that the converter can draw power from the two input sources simultaneously or separately, and it can be controlled and switched between the two operating modes flexibly.

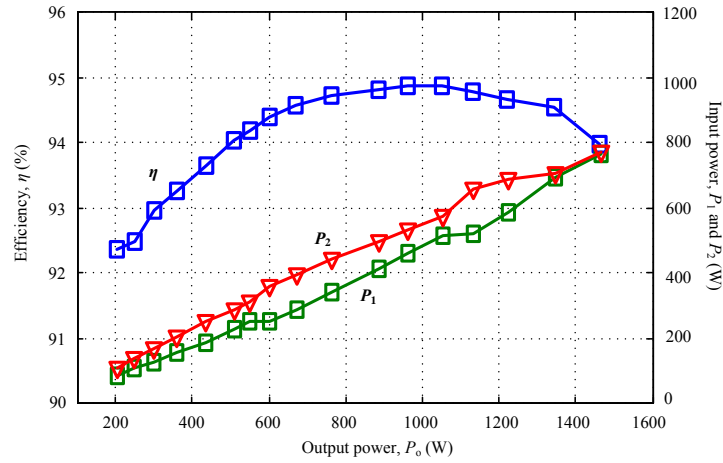
The efficiencies are measured without including the gate driver losses, and presented in Fig. 13. The efficiency curves with respective to the input voltage in the single input mode are plotted in Fig. 13(a). It exhibits a maximum efficiency of 96.5% with 50 V input, and the measured efficiency is 92.1% at 1500 W with 30 V input.

Fig. 13 (b) and (c) show the conversion efficiency when the converter operated in dual-input mode. The efficiency in this mode is defined as

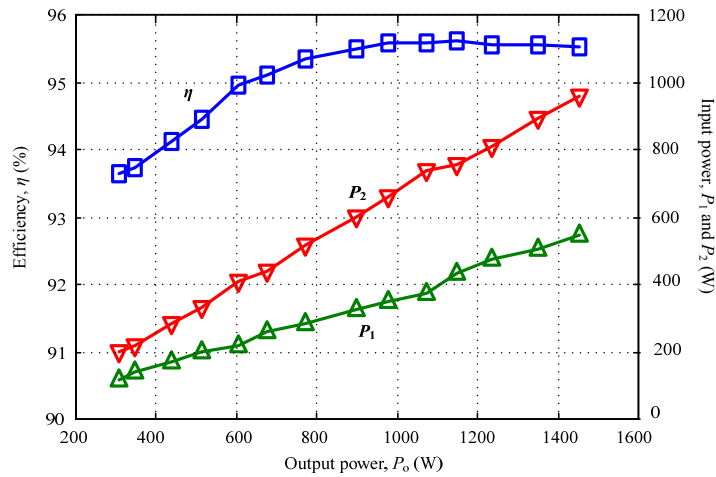
$$\eta_{dual-input} = \frac{P_o}{P_1 + P_2} \quad (18)$$



(a) Case 1: Single input power source connected;



(b) Case 2: $V_1=V_2=30$ V, and $P_1 \approx P_2$;



(c) Case 3: $V_1=50$ V, $V_2=30$ V and $P_1 \neq P_2$;

Fig. 13: Measured efficiency curves of the proposed converter.

The measured efficiency curve of the converter with the conditions: input voltages $V_1=V_2=30$ V, output voltage of 400 V, and $P_1\approx P_2$, are shown in Fig. 13 (b). Comparing to the efficiency curves shown in Fig. 13(a), in dual-input mode, the measured efficiency is about 92.4% at the output power of 200 W, which is lower than that in single-input boost mode because of higher switching losses. But at high output power, the efficiency is higher in dual-input operation mode, which is around 94.0% ($P_o=1450$ W). Fig. 13 (c) shows the measured efficiency with input voltages $V_1=50$ V, $V_2=30$ V, output voltage of 400 V, and input power $P_1\neq P_2$. The maximum efficiency is measured as 95.7%.

5. CONCLUSION

There are some solutions to the multi-input-port voltage-fed or current-fed isolated converters which can be utilized in the applications in which hybrid sustainable energy sources involved. Comparing to the existing topologies, the converter proposed in this paper has the promising points: the lower input current ripple, two controllable independent input power ports (can be extended to multiple ports), the symmetrical circuit structure which is favourable to achieving magnetic integration and modularizing. The most prominent characteristic of the proposed converter is that the main power flow path, consisting of 4 transformers and full bridge rectifier, is shared by both of the input ports, and the nominal power of each transformer and rectifier can be reduced, so a higher power density can be achieved. There are still some negative sides such as complex transformer windings connection and no common ground, and in the future research, the dc offset of transformers caused by unbalance on the voltages or the switching times has to be investigated in depth. Overall, the proposed converter is one of the promising candidate circuits, and is suitable to the applications with hybrid renewable energies.

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